



# Low-depth, compact, and error-tolerant photonic matrix-vector multiplication beyond the unitary group

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**Abstract:** Large-scale programmable photonic circuits are opening up new possibilities for information processing providing fast and energy-efficient means for matrix-vector multiplication. Here, we introduce what we believe to be a novel architecture of photonic circuits capable of implementing non-unitary transfer matrices, usually required by photonic neural networks, iterative equation solvers, or quantum samplers. Our architecture exploits compact low-depth beam-splitter meshes rather than bulky fully connected mixing blocks used in previous designs, making it more compatible with planar integrated photonics technology. We have shown that photonic circuits designed with our architecture have lower depth than their standard counterparts and are extremely tolerant of hardware errors.

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## 1. Introduction

Programmable photonic circuits are indispensable ingredients of classical [1–3] and quantum information processing devices [4,5]. For these devices to achieve the ultimate efficiencies promised by photonics, namely, accelerated speed and energy-efficiency of computation, it is necessary to use programmable interferometers capable of implementing large-scale and high-quality linear transformations. However, fabrication of programmable interferometers with the required scale and quality is challenging due to hardware errors [6–9]. Therefore, developing interferometer architectures that are less susceptible to errors, while optimally exploiting the resources of a specific photonic platform is very important and timely [10].

The fundamental mathematical operation of matrix-vector multiplication (MVM) can be efficiently performed by programmable photonics. In particular, this operation is essential for data transformation, weight adjustments, and learning processes in photonic neural networks [11]. In recent years, the development of novel architectures has been primarily focused on programmable interferometers that implement multiplications by unitary transfer matrices. In particular, the planar meshes of Mach-Zehnder interferometers (MZIs) proposed by Reck [12] and Clements [13] can implement arbitrary unitary transfer matrices. These architectures are well suited for fabrication by the mature integrated photonics technology enabling massive production of sophisticated optical circuits [14–16]. Sadly, errors in the constituent directional couplers introduce errors in the implemented multimode transformations [17]. The effect of errors can be alleviated by adding extra elements into optical circuits that correct the errors, however, this makes the circuits larger and harder to program [18]. Several error-tolerant architectures for programmable unitaries that do not require extra phase-shift elements have been proposed [19–22] and demonstrated in experiments [9,23].

A class of linear transformations broader than unitaries is usually required for photonic information processing, in particular, in classical photonic neural networks [24], iterative equation solvers [3] or quantum graph problem solvers [25]. Fortunately, one can use programmable

unitary circuits to implement these generic linear transformations. Common approaches embed the transformation in a larger unitary leading to an overhead in the circuit depth that is typically two times larger than the number of modes in the desired transformation. It turns out that this depth scaling is suboptimal [26,27].

Recently, Tang et al. [26] have shown that arbitrary transfer matrices can be implemented by programmable circuits with twice lower depths than in the aforementioned approaches. To achieve that, the authors considered a low-depth version of the architecture [20], known to be universal and exhibiting high tolerance to hardware errors. This architecture relies on static fully-connected mixing blocks requiring interaction between all participating modes at once, which is costly to accomplish, especially by planar integrated photonics technologies.

Here we propose an architecture of programmable interferometers that are simultaneously low-depth and error-tolerant. The architecture relies on partially mixing static blocks conveniently realized by a minor modification of the beam-splitter (BS) mesh, which we have studied previously as means to implement programmable unitaries [19]. The proposed programmable circuits are more compatible with planar manufacturing technologies, since they do not require multimode mixing contrary to [26]. As a result, the overall footprint, that includes both static and programmable elements, is more compact than that of the known counterparts.

The paper is organized as follows. In Sec. 2 we review the methods of constructing programmable multimode optical circuits relevant for understanding our results that follow. In Sec. 3 we introduce our architecture of programmable circuits and study its performance. We conclude in Sec. 4.

## 2. Programmable multimode optics

The transformation of a linear  $N$ -mode optical device can be described by its complex-valued  $N \times N$  transfer matrix  $U$  linking the input,  $\mathbf{a} = (a_1, \dots, a_N)^T$ , and output,  $\mathbf{b} = (b_1, \dots, b_N)^T$  amplitude vectors:

$$\mathbf{b} = U\mathbf{a}. \quad (1)$$

Multimode interferometers performing linear transformations have the form of sequence of layers, each consisting of tunable phase-shifts and static multimode blocks, as illustrated in Fig. 1(a). The transfer matrices of such interferometers can be written as

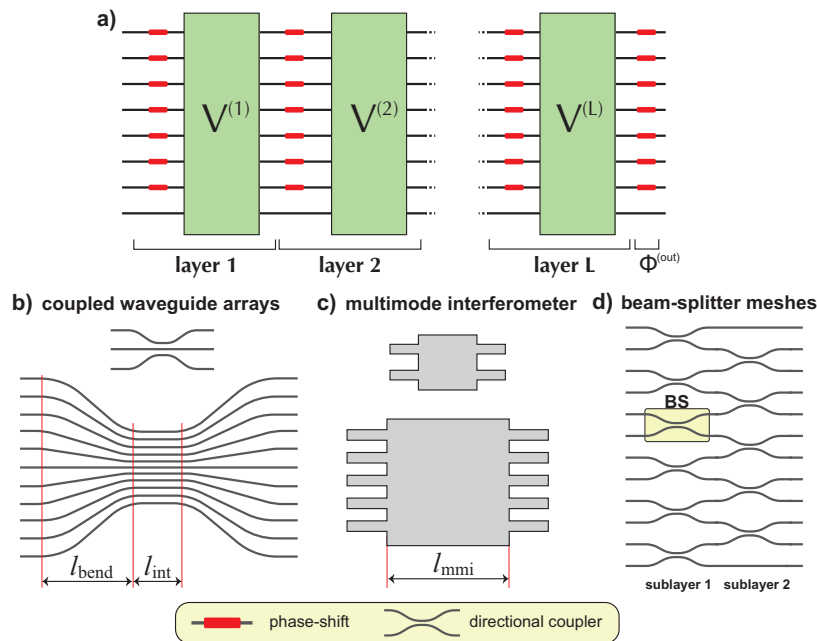
$$U = \Phi^{(L+1)}(\boldsymbol{\varphi}^{(L+1)}) \prod_{l=1}^L V^{(l)} \Phi^{(l)}(\boldsymbol{\varphi}^{(l)}), \quad (2)$$

where  $\Phi^{(l)}(\boldsymbol{\varphi}) = \text{diag}(e^{i\varphi_1}, \dots, e^{i\varphi_{N-1}}, 1)$  is the diagonal matrix of a tunable layer with index  $l$  ( $l = \overline{1, L+1}$ ) with  $\varphi_j$  being tunable phase-shifts,  $V^{(l)}$  – the transfer matrix of a static layer with index  $l$ . In the following, we consider interferometers with programmable transfer matrices, which is achieved by properly setting the tunable phase-shifts.

The transformation (2) with  $N - 1$  phase-shifts per layer corresponds to the circuit with densest possible packing of these elements. In this work, we are interested in low-depth architectures of programmable circuits and, thus, from the very beginning consider interferometers of this kind. However, it should be noted that not all programmable circuits can be reduced to the form. For example, the unitary architectures [13,19,20] can be compactified to form (2) using the method proposed in [28], whereas the architecture proposed in [22] cannot.

### 2.1. Unitary transformations

In real programmable photonic devices tunable phase-shifts are relatively large and lossy. This hinders the scaling of the programmable circuits and motivates the development of low-depth architectures. Therefore, an important parameter that should be kept in mind at designing a



**Fig. 1. Layered structure of multimode programmable circuits:** a) optical scheme consisting of  $L$  layers of interleaving static blocks  $V^{(l)}$  and tunable phase-shifts  $\Phi^{(l)}$ ; the output phase-shift layer  $\Phi^{(out)}$  is added which is not a part of the layers. Implementations of the static blocks by b) coupled waveguide arrays [20,23,26], c) planar multimode interferometers (MMI) [21], and d) beam-splitter (BS) meshes (one BS element is highlighted) [19].

programmable circuit is its depth  $D$ , which we define as the number of phase-shift layers, i.e.  $D = L + 1$ . For universal unitary architectures the minimal depth of an  $N$ -mode circuit is  $D = N + 1$ , which corresponds to the total of  $N^2 - 1$  phase-shifts — the number of real parameters necessary to describe an arbitrary  $N \times N$  unitary matrix up to a global phase.

In (2), the choice of particular static transfer matrices  $V^{(l)}$  specified by a chosen architecture, has a strong effect on the circuit functionality. For example, according to our previous work [20], error-tolerance of programmable unitaries is achieved by choosing static multimode mixing linear optics for which  $V^{(l)}$  are dense matrices. However, the experimental realizations of such transfer matrices requires organization of interference between all participating modes in each layer. As a result, the area required to allocate the circuit scales unfavorably with the size of the target transformations  $N$ , thereby limiting the size of achievable circuits. To illustrate this issue, Fig. 1(b) shows an example of a multimode mixing block implemented by coupled waveguide arrays [29,30]. The transformation performed by the coupled waveguides is governed by the coupling taking place between neighbouring waveguides, which necessitates increasing the interaction length  $l_{int}$  as  $N$  grows in order to achieve a fully mixing matrix  $V^{(l)}$ . Moreover, the bends required to couple the waveguides should have longer length  $l_{bend}$  with increasing  $N$  (see Fig. 1(b)). Another way to implement fully mixing matrices  $V^{(l)}$  by integrated photonics is using the multimode interferometers (MMI) [31], shown in Fig. 1(c). Similarly to the coupled waveguides arrays, the MMIs' length  $l_{mmi}$  scales with the size  $N$  of the programmable circuits. More sophisticated methods of designing mixing blocks in planar integrated photonics do not aid in precluding the scaling of the static blocks either [32].

As an alternative, compact circuits can be realized by another programmable unitary architecture that uses meshes of beam-splitters (BSs), which has been proposed in our previous work [19].

The corresponding static block used in this architecture is depicted in Fig. 1(d). The block consists of two BS layers, so that the static block transfer matrices read:

$$V_{\text{BS}}^{(l)} = \prod_{k \in \Omega_2} T_{\text{BS},k}^{(l,2)} \prod_{j \in \Omega_1} T_{\text{BS},j}^{(l,1)}, \quad (l = \overline{1, L}), \quad (3)$$

where

$$T_{\text{BS},j}^{(l,m)} = \begin{pmatrix} 1 & \cdots & \cdots & \cdots & \cdots & 0 \\ \vdots & \ddots & & & & \vdots \\ \vdots & & \rho_j^{(l,m)} & i\tau_j^{(l,m)} & & \vdots \\ \vdots & & i\tau_j^{(l,m)} & \rho_j^{(l,m)} & & \vdots \\ \vdots & & & & \ddots & \vdots \\ 0 & \cdots & \cdots & & & 1 \end{pmatrix} \quad (4)$$

designate the transfer matrix of a single BS acting on modes  $j$  and  $j + 1$  in the sub-layer with index  $m$  ( $m = 1, 2$ ).  $\Omega_1$  and  $\Omega_2$  denote the ordered sequence of BSs in the first and second sub-layer, respectively. The BS matrix (4) has all diagonal elements equal to one except those labeled by reflectivity  $\rho_j^{(l,m)}$ , and all off-diagonal elements equal to zero except those labeled by transmissivity  $\tau_j^{(l,m)}$  ( $\tau_j^{(l,m)2} + \rho_j^{(l,m)2} = 1$ ). Obviously, matrices (3) are radically different from the ones of the multimode mixing blocks, e.g. implemented by coupled waveguide arrays, in that they provide much lesser connectivity.

At the same time the BS-based architecture with static blocks depicted Fig. 2(c) is advantageous compared to the architecture based on multimode mixing blocks, such as those shown in Fig. 2(b). This is due to the fact that the length of the static block  $l_{\text{BS}}$  is independent on the scale of the multimode transformation  $N$ . In addition, the BS-based architecture is better suited for fabrication by intergated photonics technology, wherein it enables the creation of deeper programmable circuits as demonstrated recently in [9]. Despite having a lower degree of connectivity and experimental complexity than the architectures based on fully mixing static blocks, the BS-based architecture still offers ultimate error-tolerance [19].

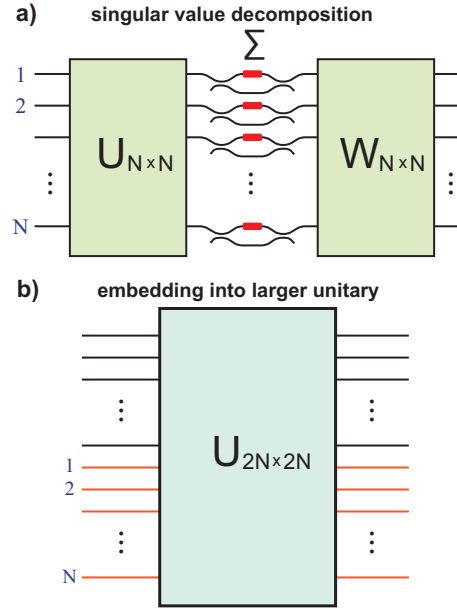
## 2.2. Transformations beyond the unitary group

Numerous applications require programmable interferometer architectures that can implement arbitrary transfer matrices beyond the unitary group. Hereinafter, we will designate such non-unitary matrices by  $A$ , in order to distinguish them.

It is known that programmable unitaries can be utilized to implement non-unitary matrices. The architectures capable of performing this task can be divided into two categories as illustrated in Fig. 2. Firstly, using a singular value decomposition (SVD) method, an  $N \times N$  matrix  $A$  can be represented as a product of three  $N \times N$  matrices:

$$A = W\Sigma U, \quad (5)$$

each of which can be implemented by optics, as shown in Fig. 2(a). Here,  $U$  and  $W$  are  $N \times N$  unitary matrices that can be implemented by any programmable unitary interferometer. The realization of the non-unitary diagonal matrix  $\Sigma = \text{diag}(\sigma_1, \dots, \sigma_N)$ , comprised of singular values  $\sigma_j$ , requires individual modulation of field amplitudes. In Fig. 2(a) this is attained by  $N$  parallel Mach-Zehnder modulators (MZIs) programmed by phase-shifts located in their arms. It should be noted that such amplitude modulation is limited to singular values  $|\sigma_j| \leq 1$ . However, it does not diminish the applicability of the SVD-based interferometers, since in photonic



**Fig. 2.** Two approaches to implement generic  $N$ -mode programmable transfer matrices  $A$ : a) singular value decomposition with two programmable  $N \times N$  unitaries  $U$  and  $W$  and one programmable diagonal  $\Sigma$ , b) embedding  $A$  into a  $2N \times 2N$  programmable unitary.

information processing devices, in particular, in photonic neural networks, scaled target transfer matrices  $A$  (e.g., divided by the maximum singular value to meet the requirements) have the same utility as the original ones. The circuit depth of the SVD-based interferometers scales as:

$$D = 2N + 3. \quad (6)$$

The second approach is based on considering a target  $N \times N$  non-unitary matrix  $A$  as being a submatrix a larger  $M \times M$  unitary one ( $M > N$ ). This embedding becomes obvious when we use the fact that any  $A$  with the singular values obeying  $|\sigma_j| \leq 1$  can be always represented as a part of a  $2N \times 2N$  unitary matrix  $U$  of the form:

$$U = \begin{pmatrix} A & \sqrt{\mathbb{I}_{N \times N} - AA^\dagger} \\ \sqrt{\mathbb{I}_{N \times N} - A^\dagger A} & -A^\dagger \end{pmatrix}, \quad (7)$$

where  $\mathbb{I}_{N \times N}$  is an  $N \times N$  identity matrix, e.g. [33]. In this approach, a straightforward method to implement arbitrary non-unitary matrices  $A$  (with singular values  $|\sigma_j| \leq 1$ ) is using a universal programmable  $2N \times 2N$  interferometer, as shown in Fig. 2(b). The circuit depth of the optical scheme scales as  $D = 2N + 2$ .

The circuit depth can be made substantially shallower than (6). As has been demonstrated in the recent paper by Tang et al. [26], arbitrary non-unitary  $N \times N$  matrices can be embedded into  $2N \times 2N$  programmable unitary circuits with depth scaling as  $D = N + 2$  — a two-fold improvement over the previously known results for complex-valued matrices. The architecture by Tang et al. [26] uses the unitary architecture depicted in Fig. 1(a) with  $L = N + 1$  multimode mixing blocks. In this work, we propose an even more compact and practical architecture.

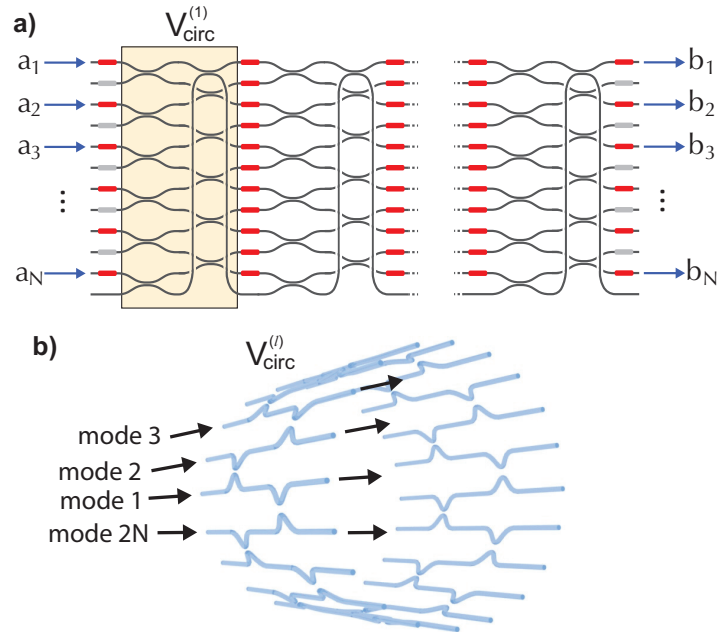
### 3. Low-depth error-tolerant architecture

The proposed architecture is illustrated in Fig. 3. Here, the constituent static blocks  $V^{(l)}$  take the form of BS meshes acting on  $2N$  modes, which are more compact than the previously used multimode mixing blocks [26]. This blocks resemble the planar meshes used in the unitary programmable architecture [19] shown in Fig. 2(d). However, there is an important modification making the circuit non-planar. Namely, there is an additional BS coupling two distant modes, thereby the whole mesh has the circular topology shown in Fig. 3(b), with the transfer matrices having the following form:

$$V_{\text{circ}}^{(l)} = \prod_{k \in \Omega_{\text{circ}}} T_{\text{BS},k}^{(l,2)} \prod_{j \in \Omega_1} T_{\text{BS},j}^{(l,1)} = T_{\text{BS},N}^{(l,2)} V_{\text{BS}}^{(l)}, \quad (l = \overline{1, L}), \quad (8)$$

where  $\Omega_{\text{circ}}$  is a sequence of BSs acting on pairs of neighbouring modes in a circular manner (see Fig. 3(b)). The sequence  $\Omega_{\text{circ}}$  is simply the sequence  $\Omega_2$  from (3) with an added BS described by the following transfer matrix:

$$T_{\text{BS},N}^{(l,2)} = \begin{pmatrix} \rho_N^{(l,2)} & 0 & \cdots & 0 & i\tau_N^{(l,2)} \\ 0 & 1 & & 0 & 0 \\ \vdots & & \ddots & & \vdots \\ 0 & 0 & & 1 & 0 \\ i\tau_N^{(l,2)} & 0 & \cdots & 0 & \rho_N^{(l,2)} \end{pmatrix}. \quad (9)$$



**Fig. 3. The proposed architecture of programmable non-unitary transfer matrices:** a) the  $N$ -mode interferometer embedded into the  $2N \times 2N$  BS mesh. One static block  $V_{\text{circ}}^{(1)}$  is highlighted. The phase-shifts in the input and output layer colored in grey are irrelevant during operation of the interferometer; b) the 3D layout of the static blocks  $V_{\text{circ}}^{(l)}$ .

As will be shown below, the seemingly minor modification of the planar BS mesh has a strong effect on the capability of the programmable circuits, especially on their tolerance to hardware errors. We notice that the modification of the planar mesh does not present an issue from the hardware perspective, since the waveguide crossings, necessary to implement the circular mesh on a planar chip, is the standard element accessible in mature integrated photonic technologies [34,35]. Moreover, modern facilities offer fabrication of multilayer photonic integrated circuits, making the proposed architecture even easier to implement [36–38].

To study the capabilities of the architecture in implementing non-unitary transfer matrices, we consider  $N \times N$  submatrices  $A$  of the transfer matrix of the  $2N$ -mode interferometer corresponding to the field amplitudes,  $a_n$  and  $b_n$ , occupying the inputs and outputs alternately, as illustrated in Fig. 3(a). To quantify the fidelity of the programmable circuits, we use the normalized square error (NSE):

$$\text{NSE}(A^{(0)}, A) = \frac{1}{N} \sum_{i,j=1}^N |A_{ij}^{(0)} - A_{ij}|^2, \quad (10)$$

which compares the target matrix  $A^{(0)}$  consisting of elements  $A_{ij}^{(0)}$  and the actual transfer matrix  $A$  consisting of elements  $A_{ij}$  realized by the interferometer, where  $N$  is the size of the matrices. Provided that the matrices  $A^{(0)}$  and  $A$  are equal, (10) gets its minimal value of  $\text{NSE} = 0$ .

Until now, we did not specify the required parameters of the programmable circuits, namely, the depth  $D$  and the values of BS's transmissivities  $\tau_j^{(l,m)}$ , corresponding to high-fidelity implementation of non-unitary transfer matrices. To find the minimal depth  $D = L + 1$  necessary to implement target matrices of given size  $N$ , we performed numerical simulations at various values of  $D$ . In parallel with this, we analyze the dependence of (10) on  $\tau_j^{(l,m)}$ 's that allowed us to investigate the error-tolerance capabilities of the circuit at specified  $N$  and  $D$ . First, we study the effect of coherent errors where all BSs are identical  $\tau_j^{(l,m)} = \tau$ , but  $\tau$  can take various values.

### 3.1. Non-unitary transfer matrices

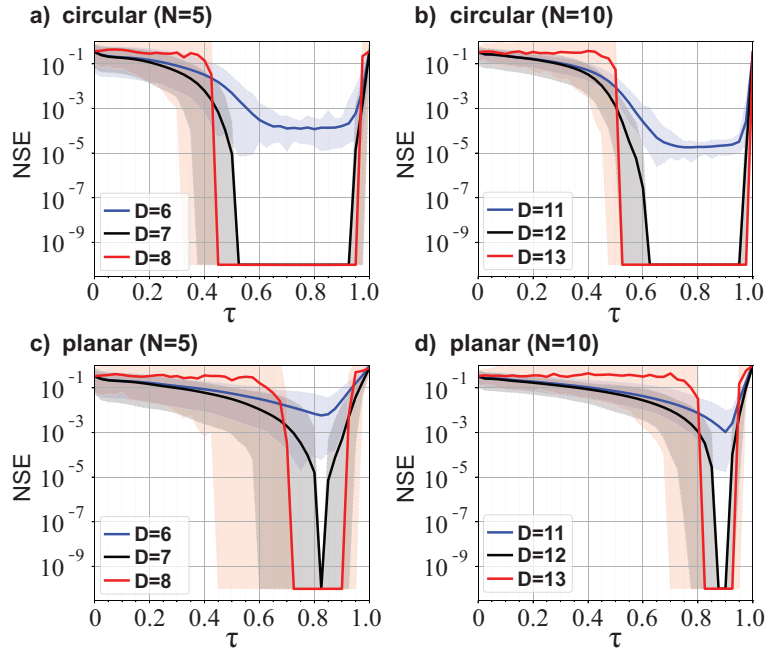
We investigate the capabilities of our architecture to implement randomly generated non-unitary matrices. We used SVD (5) to generate a target matrix  $A^{(0)}$ , wherein the unitary complex-valued matrices  $U$  and  $W$  were drawn from the Haar random distribution using the method based on the QR-decomposition of random matrices from the Ginibre ensemble [39]. The diagonal matrix  $\Sigma$  was filled with independently generated values from a uniform distribution in the  $[0, 1]$  range.

There is no known analytical solution for the values of phase shifts that minimize the fidelity measure (10), except for some specific architectures [12,13], thereby necessitating the use of a numerical optimization algorithm (see Supplement 1 for details). Given a target matrix  $A^{(0)}$ , the algorithm was searching towards a global minimum of NSE over the space of phase-shifts  $\varphi^{(l)}$  ( $l = \overline{1, D}$ ). To decrease the chance of falling into local minima, we used multiple runs of optimization ( $\sim 100$ ) with random initial values of the phases. Each numerical experiment involved optimization over a series of target matrices  $A^{(0)}$ . Using the optimization method, we studied the effect of different values of  $\tau$  on attained NSE values. In addition to the circuits with the circular BS mesh, we also conducted simulations for the circuits based on the traditional planar BS meshes (see Fig. 1(c)). Figure 4 shows the obtained dependencies of NSE on  $\tau$  for the proposed circular programmable BS meshes (Fig. 4(a,b)) and the planar programmable BS meshes (Fig. 4(c,d)). For the circuits built with the circular BS meshes, three dependencies are plotted that correspond to

1. a value of depth  $D_{\text{ET}}$  at which the circuit exhibits a high-fidelity plateau with  $\text{NSE} \approx 0$ , where a particular value of  $\tau$  does not matter,
2. a value of depth  $D_{\text{ET}} - 1$ , to demonstrate the threshold-like appearance of the  $\text{NSE} \approx 0$  plateau, and

- a value of depth  $D_{ET} + 1$ , to demonstrate further error-tolerance improvements obtained by adding one extra layer.

Specifically, for  $N = 5$  and  $N = 10$  we arrive at  $D_{ET} = 7$  and  $D_{ET} = 12$ , respectively. Therefore, this suggests that  $D_{ET} = N + 2$ , which is the same as shown in [26] for the architecture based on the multimode mixing blocks, implemented as coupled waveguides (Fig. 1(b)) or MMIs (Fig. 1(c)).



**Fig. 4.** The effect of coherent hardware errors on the performance of programmable interferometers: a) and b) the dependence of NSE on the BS transmissivity for the proposed circular programmable BS meshes at  $N = 5$  and  $N = 10$ , respectively; c) and d) the dependence of NSE on the BS transmissivity for the planar programmable BS meshes at  $N = 5$  and  $N = 10$ , respectively. The dependencies are calculated at 41 values of  $\tau$ , evenly taken in the range  $[0, 1]$ . For each  $\tau$  value the optimization has been performed over 100 randomly sampled target matrices.

Obviously, the appearance of a wide plateau of  $\tau$ 's with  $NSE \approx 0$  suggests that the programmable circuits are tolerant to hardware errors that comes in the form of deviations in the constituent static BS elements. Also notice that the  $NSE \approx 0$  plateau is so wide that the corresponding static errors in BS elements, that should fall well in this plateau, are far beyond what is likely to be encountered in practice.

We used the obtained depth values  $D_{ET} - 1$ ,  $D_{ET}$  and  $D_{ET} + 1$  to plot the corresponding dependencies for the planar BS meshes in Fig. 4(c,d). One can see that, in strike contrast to the circular BS meshes, the planar BS meshes do not exhibit the high-fidelity plateau at the threshold value  $D_{ET}$ , necessary for tolerance to hardware errors. Adding one extra layer results in the appearance of a plateau, which width, however, is narrower than that of the circular circuit at  $D_{ET}$ .

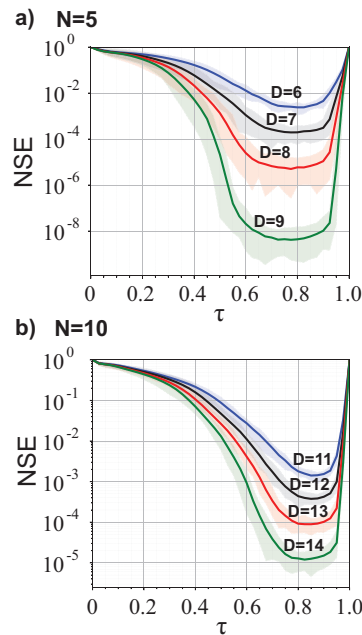
In addition to the coherent errors, assuming correlated deviations of the BS parameters, we studied the influence of incoherent BS errors. For this, we generated  $\tau_j^{(l,m)}$  independently from the gaussian random distribution for various distribution widths. The high-fidelity plateau, similar to

the case of coherent errors, is observed, thereby proving the tolerance to hardware errors of our architecture.

### 3.2. Special cases

The analysis of the capabilities of the proposed architecture on randomly sampled non-unitary matrices by no means prove its operation for arbitrary transfer matrices that can be encountered in real uses. Therefore, we have also considered a special case of transfer matrices that fall out of the analysis conducted above.

In particular, we analyse the implementation of generic unitary transfer matrices, which is also a case very unlikely to be caught by sampling non-unitary matrices of the larger size. We generated the target matrix  $A^{(0)}$  to be a unitary matrix sampled from the Haar random distribution using the method based on the QR-decomposition of random matrices from the Ginibre ensemble. As before, we used the fidelity measure (10). Figure 5(a) and Fig. 5(b) demonstrate the obtained results for unitary transfer matrices of  $N = 5$  and  $N = 10$ , respectively. As can be seen from the figures, the circular interferometer does not work in error-tolerant way, as it did for non-unitary target matrices. In addition to generic unitary matrices, we also studied the implementation of permutation matrices which are unitary, but present a more narrower class. The obtained results turned out to be similar to the ones illustrated by Fig. 5.



**Fig. 5.** The dependence of fidelity measure NSE on the BS transmissivity for the proposed circular programmable BS meshes at  $N = 5$  (a) and  $N = 10$  (b) in the case of unitary target matrix  $A^{(0)}$ . Several dependencies are plotted in the figures that correspond to the circuit depth  $D = N + 1, N + 2, N + 3$  and  $N + 4$ . The dependencies are calculated at 41 values of  $\tau$ , evenly taken in the range  $[0, 1]$ . For each  $\tau$  value the optimization has been performed over 100 randomly sampled unitary target matrices.

### 3.3. Relaxed requirements for target matrices

To achieve high-fidelity matrix-vector multiplication by programmable photonic circuits in general and our circular architecture, in particular, we suggest the following trick. In many

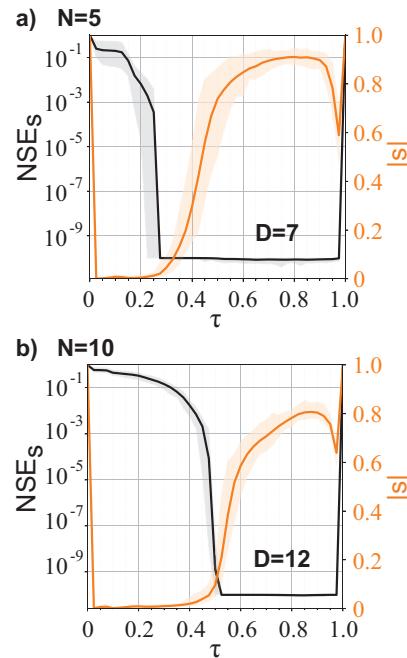
applications, matrix-vector multiplication is allowed to be performed up to a global complex value  $s$ . In other words, multiplication by the matrix  $sA^{(0)}$  can be as useful as multiplication by the specified one  $A^{(0)}$ . For example, this is usually the case in opto-electronic devices [1,3], wherein the vector result of the photonic multiplication is immediately measured and converted to electronic format for further processing. The scaling operation present a simple routine, which can be easily performed by electronics.

We used the modified fidelity measure that takes into account the freedom of scaling factor:

$$\text{NSE}_s(A^{(0)}, A) = \frac{1}{|s|^2} \text{NSE}(sA^{(0)}, A), \quad (11)$$

which we optimize in the space of phase-shifts  $\{\varphi^{(l)}\}$  and the scaling factor  $s$  (see [Supplement 1](#) for details). It should be noted that, because lower values of  $|s|$  are associated with higher losses introduced to the transformation, higher  $|s|$  are usually preferable. Our optimization algorithm used to minimize (11) opts for higher values of  $|s|$ .

We challenge our architecture again in the task of implementing unitary transfer matrices. The results obtained in optimization of (11) are shown in Fig. 6. Comparing these results with those shown in Fig. 5, we see the significant effect of using the relaxed fidelity measure (11) on the quality of implemented unitary matrices. The high-fidelity plateau with  $\text{NSE}_s \approx 0$  is observed, which suggests the tolerance to hardware errors.



**Fig. 6.** The dependence of the scaled NSE fidelity measure and the absolute value of the matrix scaling factor  $|s|$  on the BS transmissivities  $\tau$  in the proposed programmable BS meshes at  $N = 5$  (a) and  $N = 10$  (b). The dependencies are calculated at 41 values of  $\tau$ , evenly taken in the range  $[0, 1]$ . For each  $\tau$  value the optimization has been performed over 100 randomly sampled unitary target matrices.

High fidelity achieved in our circular interferometers may be somewhat compromised by the inherent imperfections present in real-world photonic devices [13,19]. In particular, the waveguide crossers required to implement our architecture on a single-layer planar integrated

chip can introduce unbalanced losses into the static blocks, thereby reducing the overall fidelity. However, waveguide crossers with losses as low as 0.008 dB have been demonstrated [34,35,40]. Additionally, if the loss levels are known prior to fabricating the device, compensating elements can be incorporated into the design to mitigate these losses. Moreover, while single-layer planar circuits are currently the focus, advances in multilayer chip fabrication technologies are expected to address the issue of unbalanced losses more effectively [36–38].

#### 4. Conclusion

In this work we proposed a novel architecture of programmable circuits capable of implementing transfer matrices beyond the unitary group. Our architecture has the advantage of having a lower depth than the previously known counterparts and possess tolerance to hardware errors. In addition, the programmable circuits designed with the architecture is compatible with planar integrated photonics. All these properties, simultaneously offered by our architecture, facilitate the fabrication of large-scale programmable circuits performing photonic matrix-vector multiplication by mature integrated photonics technologies. Taking into account the typical scale of matrix-vector multiplications required by modern computing, in particular, deep neural networks, the advantages of our circuits are decisive for practical implementation in real-world computing systems. This makes us believe that the results of this work are of interest for both fundamental and applied fields.

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**Disclosures.** The authors declare no conflicts of interest.

**Data availability.** Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

**Supplemental document.** See [Supplement 1](#) for supporting content.

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